This application claims the benefit of co-pending commonly-owned U.S. Patent [Provisional] Application Serial No. [_____] 10/033,027, (attorney docket number [CYPR-C00232] CYPR-CD00232), filed October 22, 2001, entitled "PROGRAMMABLE MICROCONTROLLER [PROGRAMMABLE SYSTEM ON A CHIP"] ARCHITECTURE," which is hereby incorporated by this reference.

Please replace the paragraph beginning at page 1, line 10 with the following:

Embodiments of the present invention generally relate to the field of integrated circuit chips. More specifically, embodiments of the present invention pertain to a system and method for dynamically reconfiguring a programmable integrated circuit [system on a chip].

Please replace the paragraph beginning at page 5, line 5 with the following:

What is required is a system and method of dynamically reconfiguring a programmable integrated circuit [system on a chip] in a convenient and efficient manner.

Please replace the paragraph beginning at page 6, line 2 with the following:

The present invention is a system and method providing dynamic programmability of an electronic device (e.g., a programmable integrated circuit [system on a chip]) in a convenient and efficient manner. In one embodiment of the present invention, the dynamic programmability enables operationally smooth (e.g., "on the fly") changes in the configuration and/or functionality of the electronic device with minimal or no disruptions to device operations. In one exemplary embodiment, the present invention is implemented in an integrated microcontroller with components that are dynamically programmable to provide different configurations and functions. A plurality of different configuration images are utilized to define the different configurations and functions and facilitate allocation of programmable components included in the electronic device accordingly.

Please replace the paragraph beginning at page 7, line 8 with the following:

In one embodiment of the present invention, the configuration and functionality of an electronic device is defined by a configuration image loaded in a memory of the electronic device. The configuration image includes instructions and data for implementing the configuration and functions. In one embodiment, a plurality of configuration images facilitate dynamic reconfiguration of a programmable integrated circuit [system on a chip] ([PSoC] e.g., a PSOC™ microcontroller, available from Cypress MicroSystems, Bothell, Washington). In one exemplary implementation of the present invention, a configuration image includes user module personalization data (e.g., [PSoC] a configuration table), module parameterization data, application program interface (API) data and user program code. Based upon the existence of a predetermined condition, the [PSoC] integrated circuit is automatically reconfigured by activating different configuration images. In one embodiment, activating different configuration images results in different values being loaded in configuration registers of functional circuit blocks included in the [PSoC] integrated circuit.

Please replace the paragraph beginning at page 8, line 5 with the following:

Figure 2A is a block diagram of one embodiment of a [PSoC] functional component depicted in greater detail.

Please replace the paragraph beginning at page 8, line 10 with the following:

Figure 3 is a flow chart of a [PSoC] dynamic configuration method, one embodiment of the present invention.

Please replace the paragraph beginning at page 8, line 12 with the following:

Figure 4 is a flow chart of a [PSoC] design tool process illustrating exemplary steps used by a design tool in accordance with one embodiment of the present invention.

Please replace the paragraph beginning at page 10, line 21 with the following:

The present invention is a system and method of dynamically programming [a system on a chip (PSoC)] an integrated circuit. In one embodiment of the present invention, a system integrated on a single substrate is dynamically programmable to provide a plurality of configurations and functionalities. In one exemplary implementation of the present invention, a plurality of configuration images defining different configurations and functionalities of a [PSoC] programmable integrated circuit are stored in a memory included in the [PSoC] programmable integrated circuit. The configuration image data may be generated and loaded on the [PSoC] programmable integrated circuit in various manners including by an electronic device design tool. In one embodiment, the electronic device design tool comprises a [device editor] configuration interface for defining user module personalization and parameterization, an automated code generator for generating source code (e.g., application program interface code), [an application editor] a source code editing interface for editing the automatically generated code, and a [debugger] debugging interface for assisting debugging operations through emulation of the target [PSoC] device. The exemplary embodiments described herein (e.g., a microcontroller) are not meant to limit the application of the present invention to any specific integrated circuit device or type (e.g., a microcontroller) and embodiments of the present invention may be implemented in a variety of integrated circuits.

Please replace the paragraph beginning at page 11, line 16 with the following:

Figure 1 is a block diagram showing a high level view of an exemplary integrated circuit (e.g., a microcontroller) 10 upon which embodiments of the present invention may be implelmented. In one embodiment, integrated circuit 10 includes a communication bus 11, static random access memory (SRAM) 12, central processing unit (CPU) 14, flash read-only memory (ROM) 15, input/output (I/O) pin(s) 18 and [PSoC] functional component 25. Communication bus 11 is electrically coupled to static random access memory (SRAM) 12, central processing unit (CPU) 14,

flash read-only memory (ROM) 15, input/output (I/O) pin(s) 18 and [PSoC] functional component 25. Static random access memory (SRAM) 12 stores volatile or temporary data during firmware execution. Central processing unit (CPU) 14 processes information and instructions. Flash read-only memory (ROM) 15 stores information and instructions (e.g., firmware). In one embodiment of the present invention, flash read-only memory (ROM) 15 stores configuration image data. Input/output (I/O) pin(s) 18 provides an interface with external devices (not shown). [PSoC functional] Functional component 25 is programmable to provide different functions and configurations.

Please replace the paragraph beginning at page 12, line 11 with the following:

It is appreciated that integrated circuit 10 is readily adaptable to include a variety of other components. In one exemplary implementation, integrated circuit 10 also includes a dedicated functionality internal peripheral component 17 which is coupled to system bus 11 in addition to the [PSoC] functional component 25. An optional test interface (TI) may be coupled to integrated circuit 10 via a test interface coupler (TIC), which may be detachable, to perform debugging operations during startup and initialization of the integrated circuit. In one embodiment of the present invention, additional functions such as clocking and power control are provided by a variety of components including a precision oscillator and phase locked loop (PLL), a voltage reference, a 32 kHz crystal oscillator (which may be utilized for a variety of applications such as calibration and synchronization, etc.), an interrupt controller (for generating interrupt signals as required), a power on reset control unit (for performing functions related to power supply stability), and a brown-out detection unit (which detects substandard, subnominal power system parameters).

Please replace the paragraph beginning at page 13, line 5 with the following:

Referring to Figure 2A, an embodiment of [PSoC] functional component 25 is depicted in greater detail. In this embodiment, [PSoC] functional component 25 includes an analog functional block 230, a digital functional block 240, and a programmable interconnect 250. In one exemplary implementation, analog functional block 230 includes a matrix of interconnected analog functional blocks A1 through AN. The number N may be any number of analog functional blocks. Likewise, digital block 240 includes a matrix of interconnected digital functional blocks D1 through DM. The number M may be any number of digital functional blocks.

Please replace the paragraph beginning at page 14, line 11 with the following:

The present invention is readily adaptable for use with numerous functional blocks that are programmably configurable to provide a variety of functions. Exemplary functional peripherals include timers, controllers, serial communications units, Cycle Redundancy Check (CRC) generators, Universal Asynchronous Receiver/Transmitters (UARTs), amplifiers, programmable gain [components ,] components, digital to analog converters, analog to digital converters, analog drivers, and various filters (e.g., high-, low-, and band-pass). In one exemplary implementation higher order user modules (e.g., modems, complex motor control, sensor devices, etc.) are created with combinations of functional blocks. Co-pending commonly-owned incorporated U.S. Patent [Provisional] Application Serial No. [_____] 10/033,027, (attorney docket number [CYPR-C00232] CYPR-CD00232), filed October 22, 2001, entitled "PROGRAMMABLE MICROCONTROLLER [PROGRAMMABLE SYSTEM ON A CHIP"] ARCHITECTURE," includes additional details on exemplary implementations of present invention integrated circuits (e.g., integrated circuit 10) and [PSoC] functional components (e.g., [PSoC] functional component 25).

Please replace the paragraph beginning at page 15, line 16 with the following:

In one embodiment of the present invention, a [PSoC] functional component (e.g., [PSoC] functional component 25) includes registers that are programmably configurable to store configuration data that defines the combination (e.g., electrical coupling) of the functional blocks and the characteristics (e.g., parameters) of the respective functional block elements. When a value is changed in a configuration register, the configuration [and or] and/or functionality of a corresponding integrated system 10 component is changed accordingly. In one exemplary implementation of the present invention, some functional blocks are configured to affect autonomous system operations, such as interrupts.

Please replace the paragraph beginning at page 17, line 15 with the following:

In the present exemplary embodiment, programmable interconnect 250 comprises a configuration system and a global mapping system. The configuration system is coupled to communication bus 11 and the global mapping system, which in turn is coupled to [PSoC] functional component 25. The configuration system is programmably configurable to selectively couple with communication bus [25] 11 and/or the global mapping system. The global mapping system facilitates selective coupling of functional blocks included in [PSoC] functional component 25 to other functional blocks and/or pin count of a pin-by-pin configurable I/O port (e.g., I/O pin(s) 18) may vary from one application to another, depending on the system device under consideration. An I/O routing modality incorporating features of the present embodiment enables flexibly configurable I/O ports to establish a specific pin locale or pin for the conveyance of particular external signals (e.g., to or from an external device) on pin by pin basis, greatly enhancing user convenience and system applicability.

Please replace the paragraph beginning at page 19, line 8 with the following:

In one embodiment of the present invention, a system timing block is included to provide timing information used for synchronizing and otherwise effectuating interfacing between system functionalities (e.g., [PSoC] functional blocks). The system timing block like the [PSoC] functional component 25 is programmable. Advantageously, this allows the system timing block to generate a myriad of different time bases, as required for any particular application the system is being configured to effectuate. These time bases may be fed into analog functional blocks and digital functional blocks for use therein, via the programmable interconnect. Examples of analog functions requiring such time bases include conversions, modulations, and the like. One striking example of a digital function requiring such time bases is a universal asynchronous receiver transmitter (UART) functionality.

Please replace the paragraph beginning at page 19, line 20 with the following:

In one embodiment of the present invention, the configuration and functionality of an electronic device (e.g., a [PSoC component] programmable integrated circuit) is defined by a configuration image loaded in a memory of the electronic device (e.g., microcontroller 10). In one exemplary implementation of the present invention, a plurality of images are loaded in a memory of an electronic system to facilitate dynamic reconfiguration of the electronic system (e.g., a [PSoC] programmable integrated circuit). The information comprising the configuration image may be represented in varying degrees of abstraction. At a low level of abstraction the configuration image is represented by source code (e.g., assembly or machine language) stored as logical values (e.g., logical ones and zeroes) in a memory (e.g., in the [PSoC] programmable integrated circuit). At a higher lever of abstraction the configuration image is represented by textual definitions or graphical images (e.g., in a design tool).

Please replace the paragraph beginning at page 20, line 11 with the following:

In one exemplary implementation of the present invention, a configuration image includes user module personalization data (e.g., [PSoC] a configuration table), module parameterization data, application program interface (API) information and user program code. The user module personalization data includes information defining the functionality and configuration of a component included in a [PSOC] programmable integrated circuit (e.g., a functional block). The parameterization data defines parameters for the [PSOC] programmable component. The API defines an operation of the [PSOC] programmable component [(e.g.,,] (e.g., apply power, remove power, sample rate of an AC to DC converter, etc.). In one embodiment of the present invention an API includes code for a function call (e.g., from a user program) and/or an interrupt. In one exemplary implementation of the present invention, user module personalization data defines an analog function block to function as an op amp, the parameterization data defines the gain of the op amp (e.g., 8X), and the API code defines a reset of the op-amp.

Please replace the paragraph beginning at page 21, line 4 with the following:

A dynamically programmable electronic device (e.g., a [PSoC] programmable integrated circuit) of the present invention is programmably configurable to perform a plurality of functions for a variety of applications. Each configuration image loaded in a present invention [PSoC] device enables the [PSoC] device to provide a different configuration and functionality. In one exemplary implementation, a present invention [PSoC] device is included in a wireless communication device (e.g., a walkie-talkie). When a transmission indication exists (e.g., a "talk" button is engaged) a first image loaded in the [PSoC] present invention device is activated (e.g., configuration registers are loaded in accordance with the first image) causing the [PSoC] components therein to perform as a transmitter and when a receiving indication exists (e.g., the talk button is not engaged) a second image loaded in the [PSoC] present invention device is activated causing the [PSoC] components therein to perform as a receiver. In another exemplary implementation, a present invention [PSoC]

device is included in a vending machine. During normal operating hours a first image loaded in the [PSoC] present invention device causes the [PSoC] components therein to participate in normal vending operations (e.g., monitoring money collection, calculating change, controlling product dispensing, etc.) and at predetermined short [duration] durations a second image loaded in the [PSoC] present invention device causes the [PSoC] components therein to participate in inventory activities (e.g., calculating the totals of products sold, determining need for additional products, participating in modem operations to communicate with a central resource, etc.)

Please replace the paragraph beginning at page 22, line 11 with the following:

Figure 3 is a flow chart of [PSoC] dynamic configuration method 300, one embodiment of the present invention. [PSoC dynamic] Dynamic configuration method 300 facilitates dynamic configuration of a [PSoC] programmable system to provide different configurations and functions. In one embodiment of the present invention, [PSoC] dynamic configuration method 300 utilizes a plurality of configuration images loaded in a [PSoC] system memory to facilitate different configurations and implement different functionalities. In one embodiment of the present invention, [PSoC] dynamic configuration method 300 facilitates configuration changes (e.g., reconfiguration) with smooth operational transitions ("on the fly") to efficiently and flexibly address differing functional or configuration requirements of end use applications. In one embodiment of the present invention, the configuration images are provided by a design tool (e.g., a computer implemented software [PSoC] design tool). Additional details on an exemplary implementation of a present invention design tool are set forth in co-pending commonly-owned United States Patent Application Serial No. [_____] 09/989,570, filed [_____2001] November 19, 2001 (attorney docket number CYPR-CD01167M), entitled "METHOD FOR FACILITATING MICROCONTROLLER PROGRAMMING", which is hereby incorporated by this reference, and United States Patent Application Serial No. [_____] 09/989,819, filed [_____2001] November 19, 2001 (attorney

docket number CYPR-CD01181M), entitled "A SYSTEM AND METHOD FOR CREATING A BOOT FILE UTILIZING A BOOT TEMPLATE", which is also hereby incorporated by this reference.

Please replace the paragraph beginning at page 23, line 12 with the following:

In step 310 a plurality of configuration images are loaded in a [PSoC] memory. In one exemplary implementation of the present invention, different configuration images define different functions and configurations for components of a target [PSoC] device. In one embodiment of the present invention, two different configuration images include copies of the same user code and in an other embodiment of the present invention two different configuration images [included] include a "call" to the same user code. In one embodiment of the present invention, each configuration image includes information associated with selections of [users] user modules for each one of the plurality of configuration images, allocations of hardware resources of the [PSoC] device to the selected user modules, parameterizations for the selected user modules, and connections between the selected user modules and to other [PSoC] device components (e.g., external pins).

Please replace the paragraph beginning at page 24, line 3 with the following:

In step 320 a [PSoC] device is configured in accordance with a first configuration image. In one embodiment of the present invention, information from the first configuration image is automatically loaded into configuration registers in the target [PSoC] device. In one exemplary implementation, the first configuration image is automatically loaded into configuration registers in response to a first condition (e.g., a talk button is activated, at a particular time, etc.).

Please replace the paragraph beginning at page 24, line 16 with the following:

In step 340 a [PSoC] device is reconfigured in accordance with a second configuration image. In one embodiment of the present invention, information from a second configuration image is automatically loaded into configuration registers in the target [PSoC] device and replaces the information associated with the first configuration image. In one exemplary implementation, the second configuration image is automatically loaded into configuration registers in response to a second condition (e.g., a talk button is not activated, at a different particular time, etc.).

Please replace the paragraph beginning at page 25, line 11 with the following:

In one embodiment of the present invention, configuration images are provided by an electronic device design tool (e.g., [a PSoC] an integrated circuit design tool). Figure 4 is a flow chart of [PSoC] design tool process 400 and illustrates exemplary steps used by a design tool in accordance with one embodiment of the present invention. [PSoC design] Design tool process 400 facilitates configuration, programming, building, emulation and debugging of a customized [PSoC] integrated circuit (a "target device"). In one exemplary implementation the [PSoC] integrated circuit is similar to integrated circuit 10 of Figure 1 with a [PSoC function] functional component 25 similar to Figure 2A.

Please replace the paragraph beginning at page 26, line 1 with the following:

In one embodiment, [PSoC] design tool process 400 is carried out by a computer system under the control of computer-readable and computer-executable instructions directed at implementing [PSoC] design tool process 400. One embodiment of an exemplary computer system utilized to implement [PSoC] design tool process 400 is set forth in incorporated United States Patent Application Serial No. [_____] 09/989,570, filed [_____2001] November 19, 2001 (attorney docket number CYPR-CD01167M), entitled "METHOD FOR FACILITATING MICROCONTROLLER PROGRAMMING". The computer-readable and computer-executable

instructions reside, for example, in data storage features of the computer system such as a computer usable volatile memory, computer-usable non-volatile memory and/or data storage device. The computer-readable and computer-executable instructions direct the computer system operation (e.g., a processor) in accordance with [PSoC] design tool process 400.

Please replace the paragraph beginning at page 26, line 15 with the following:

In step 410, an interface for user interaction is provided. In one embodiment of the present invention, the interface is provided for selecting applicable "user modules" (e.g., a preconfigured function that may be based on more than one [PSoC] functional block). In one exemplary implementation, a user module when programmed and loaded on a memory of the [PSoC] device directs a functional block to work as a peripheral on the target device. At any time in [PSoC] design tool process 400, user modules may be added to or removed from the target device. The selected user modules are associated with (e.g., "placed" or "mapped to") representations of [PSoC] functional blocks defined in the [PSoC] design tool. Once a user module is associated with a [PSoC] representation, its parameters can be viewed and modified as needed. Global parameters used by a plurality of user modules (for example, CPU clock speed) can also be set. In one embodiment of the present invention, interconnections between selected user modules are specified (e.g., either as each user module is placed or afterwards). The pin-out for each [PSoC] block can also be delineated, making a connection between the software configuration and the hardware of the target [PSoC] device.

Please replace the paragraph beginning at page 27, line 15 with the following:

In step 430, programming of the desired functionality into the target device is facilitated. In one embodiment of the present invention, source code files can be edited, added or removed. In one

embodiment of the present invention, programmable configuration of external [PSoC] ports is also facilitated by [PSoC] design tool process 400.

Please replace the paragraph beginning at page 28, line 6 with the following:

In step 450 the target device is "built" within the [PSoC] design tool. Building the target device in the [PSoC] design tool includes linking the programmed functionalities of the source files (including device configuration). In one exemplary implementation of the present invention, the linked programmed functionalities and the source files are downloaded to an emulator for debugging in step 450.

Please replace the paragraph beginning at page 28, line 16 with the following:

In step 470 a configuration image generated using [PSoC] design tool process 400 is loaded into memory of a [PSoC] target device. In one embodiment of the present invention a plurality of configuration images are loaded into memory of a [PSoC] target device.

Please replace the paragraph beginning at page 29, line 1 with the following:

Although specific steps are disclosed in [PSoC] design tool process 400 of Figure 4, such steps are exemplary. That is, the present invention is well suited to use with various other steps or variations of the steps recited in process 400. Additionally, for purposes of clarity and brevity, the discussion is directed at times to specific examples. The present invention [PSoC] design tool process 400, however, is not limited solely to use to design a particular target device (e.g., [a PSoC device] an integrated circuit and/or microcontroller). Instead, the present invention is well suited to use with other types of computer-aided hardware and software design systems in which it may be necessary to accomplish a multitude of tasks as part of an overall process directed at designing an electronic device.

Please replace the paragraph beginning at page 29, line 12 with the following:

Thus, the present invention provides convenient and efficient dynamic configuration of an electronic device (e.g., [a PSoC] an integrated circuit). An electronic device design of the present invention facilitates dynamic programmability that enables operationally smooth (e.g., "on the fly") changes in the configuration and/or functionality of the electronic device with minimal or no disruptions to device operations. The present invention allows utilization of the same components to perform different functions and take on different configurations that are capable of satisfying the requirements of different applications. A variety of functions and [configuration] configurations may be implemented with less resources than traditional systems. The present invention does not require duplicative resources (e.g., circuit [components)] components) for dedication to the performance of different functions or configurations. A present invention dynamically programmable device design also facilitates utilization of device components that would otherwise be operationally idle.

IN THE CLAIMS

Please amend the claims as follows:

2. (AMENDED) The circuit of Claim 1, wherein said programmable [system on a chip] functional component includes:

a programmable interconnect for coupling components to said bus;

an analog functional block configurable to perform analog functions, said analog functional block coupled to said interconnect; and

a digital functional block configurable to perform digital functions, said digital functional block coupled to said interconnect.

12. (AMENDED) The electronic device dynamic configuration method of Claim 10 wherein said electronic device is a programmable [system on a chip (PSoC)] integrated circuit.

IN THE DRAWINGS

Applicant respectfully requests approval of the drawing changes proposed in the enclosed Request for Approval of Drawing Changes.

SUPPORT FOR AMENDMENTS

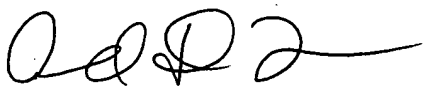
Support for the amendments herein can be found throughout the specification, claims and Figures as originally filed (e.g., page 1, lines 10-13; page 6, lines 8-10; page 7, lines 8-13 and 19-21; page 10, lines 21-24; page 11, lines 5-21; page 12, lines 11-15; page 13, lines 6-13; page 14, lines 11-13; page 14, line 20 through page 15, line 7; page 15, line 16 through page 16, line 4; page 19, lines 8-14; page 20, lines 2-4; page 25, lines 11-17; page 26, lines 15-22; page 27, lines 1-9 and 15-19; page 28, lines 1-15; page 29, lines 1-11; claims 1-2; and Figures 1 and 4) and in copending, incorporated U.S. application serial nos. 09/989,570 and 10/033,027. The present amendment intends to clarify references to a trademark of Cypress MicroSystems, Inc. (see, e.g., M.P.E.P. § 608.01(v) and the attached printouts from http://tess.uspto.gov/, notably the "PSOC" trademark registration information therein, and http://www.cypressmicro.com/corporate/CY_Announces_nov_13_2000.html.). No new matter is introduced.

REMARKS

Claims 1-21 are presented for consideration in the present application, which is now believed to be in condition for examination. Early notice to that effect is earnestly solicited.

Respectfully submitted,

WAGNER, MURABITO & HAO LLP



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Goods and Services	IC 009. US 021 023 026 036 038. G & S: semiconductors devices; microprocessors; and integrated microelectronic devices in the nature of semiconductors devices
Mark Drawing Code	(1) TYPED DRAWING
Serial Number	75951037
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CYPRESS MICROSYSTEMS UNVEILS PROGRAMMABLE SYSTEM-ON-A-CHIP FOR EMBEDDED INTERNET, COMMUNICATIONS AND CONSUMER SYSTEMS

PSoC™ Devices Integrate Programmabl Analog and Digital Functions To Simplify D sign Of Wireless, Handheld, Data Communicati ns, and Industrial Systems

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WOODINVILLE, Wash., November 13, 2000 - Cypress MicroSystems, a subsidiary of Cypress Semiconductor, today introduced a family of programmable system-on-a-chip (PSoC™) devices, designed to implement a single, configurable device on MCU-based system boards. As general purpose solutions, PSoC devices are targeted for implementation in embedded applications, including audio, wireless, handheld, data communications, Internet control, industrial, and consumer systems.

PSoC devices integrate a fast microcontroller, SONOS™-based (Silicon Oxide Nitride Oxide Silicon) Flash memory and SRAM, and programmable arrays of analog and digital system functions - known as PSoC blocks - in low-cost, small-footprint packages. To save designers time, Cypress Microsystems also offers User Modules - pre-designed peripherals comprised of PSoC blocks. By selecting a PSoC with the needed resource combination of memory, PSoC blocks and pins, designers have a device that reduces costs by eliminating external chips and simplifying system design.

"Today there are thousands of different 8-bit microcontrollers on the market, and designers still have trouble finding one that is a perfect fit for their application. In addition, embedded applications require analog peripherals that usually call for additional external devices," said Mike Polen, Cypress MicroSystems's vice president of marketing. "Engineers know that the perfect solution is a custom-designed system-on-a-chip, but custom microcontrollers, ASICs and PLDs are expensive, require very large volumes or call for specialized design skills."

"In contrast, the Cypress Microsystems PSoC solution offers custom configurations, takes no time or special expertise to create, incurs no NRE, and integrates both analog and digital functions," continued Polen. "These factors make the cost of the PSoC solution competitive with standard microcontrollers."

SONOS - a proprietary Cypress process technology - is key to Cypress Microsystems's system-on-a-chip. SONOS is a cost-effective, electrically-erasable, programmable, non-volatile memory structure that speeds time-to-market at a cost that is comparable with commodity devices. SONOS is also being implemented in Cypress Semiconductor's frequency timing generators, USB controllers and intelligent control network devices.

About PSoC blocks and User Modules

After a review of the peripherals found in microcontrollers and the analog ICs used in typical designs, Cypress Microsystems engineers selected a variety of digital and analog peripherals, then created PSoC blocks, or system-on-a-chip blocks, and integrated them into each PSoC device. Users select the functions they need and configure the PSoC blocks on the PSoC device accordingly.

Digital PSoC blocks are 8-bit peripherals that can be programmed to perform a variety of functions by changing the contents of a few registers. They can be configured as timers, controllers, serial communications ports, CRC generators, or pseudo-random number generators. They can be connected in series to handle more complex functions - for example, a 24-bit timer is three connected 8-bit PSoC blocks acting as timers.

Analog PSoC blocks consist of programmable operational amplifier circuits that can be configured to perform a set of typical analog peripheral functions. Analog PSoC blocks can be programmed by setting a few registers to interconnect and trim the appropriate operational amplifier circuit to create the desired result. Among the typical peripherals that can be created are amplifiers, DACs, ADCs, analog drivers, and high-, low- and band-pass filters.

To eliminate the need for customers to understand PSoC blocks in-depth and further shorten development time, Cypress Microsystems developed User Modules, preconfigured peripherals created from PSoC blocks. User Modules allow customers to select the functions they need and automatically integrate the necessary PSoC

blocks into their PSoC device.

Software Support

Cypress Microsystems will offer PSoC Designer™, a complete development system to support the PSoC device. The system will include a C compiler and assembler, a linking and debugging tool, an in-circuit emulator, and the Device Editor™.

Designers can use the Device Editor and its graphical interface to configure a PSoC device by dragging the desired peripherals or functions - from a library of User Modules - into the part. The selected User Modules are then automatically mapped onto the available PSoC blocks.

On-chip Flash program memory stores each PSoC device's parameters, allowing the user to reprogram the device during production, during system test or in the field. PSoC devices may even be self-reprogrammed remotely.

"PSoC devices are like a screwdriver with replaceable bits," stated Nathan John, Cypress Microsystems's director of marketing. "They can be configured and reconfigured as the design progresses and functional requirements change. They provide a core set of analog and digital functions that eliminate the need for additional devices. And they can be programmed to custom-fit any application."

Availability and Pricing

Cypress Microsystems will initially offer the following PSoC devices:

Part Number	Max. Speed	Package	Samples	Production	Price (Q 1,000)
CY8C25122	24 MHz	8-pin DIP	Q1 2001	Q1 2001	$ 1.76
CY8C26233	24 MHz	20-pin DIP 20-pin SOIC 20-pin SSOP	Q1 2001	Q1 2001	$ 2.21
CY8C26443	24 MHz	28-pin DIP 28-pin SOIC 28-pin SSOP	Q4 2000	Q1 2001	$ 2.79
CY8C26643	24 MHz	48-pin DIP 48-pin SSOP 48-pin TQFP	Q1 2001	Q1 2001	$ 3.53

About Cypress Microsystems

Cypress Microsystems designs, develops, manufactures and markets high-performance, field programmable integrated micro-based solutions for high-volume embedded control functions in computer, communications, consumer and control applications. Established as a subsidiary of Cypress Semiconductor Corporation in the fourth quarter of 1999, Cypress Microsystems's stockholders are its employees and Cypress Semiconductor. The close association with Cypress Semiconductor allows access to their process and design technology, and field sales and applications forces. Cypress Microsystems is based near Seattle in Woodinville, Washington.

The Cypress Microsystems PsoC™ family of programmable system-on-a-chip devices will replace many MCU-based system boards with one single-chip, programmable PSoC. A single PSoC device provides a fast microcontroller, SONOS™ FLASH and SRAM memory, and configurable analog and digital peripheral blocks in a range of convenient pin outs and memory sizes. This new product family will bring the cost and time-to-market advantages of programmable technologies, such as CPLDs and FPGAs, to the emerging system-on-a-chip marketplace.

More information about Cypress Microsystems and its products can be accessed through its Web site at www.cypressmicro.com.

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